Name : **Dr. Shyam Kishore G**
Qualification : **Ph.D, M.Tech(VLSI Design), B.Tech(ECE)**
Category : **BC-B**
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Conferences / Journals:

1. MSS Lakshmi Lavanya, A Mounika Rajeswari, G Shyam Kishore, (2025), "Classification Method for Geographic Labeling of Web Objects', 15th International Conference on Soft Computing and Pattern Recognition (SoCPaR 2023): Volume 2, vol. 1245.
2. G. S. Kishore, Y. L. Kumar, K. S. Abhilash and E. Aparna, "A Bitwise Operations-Based Image Steganography Technique for LSB Replacement," 2024 1st International Conference on Sustainable Computing and Integrated Communication in Changing Landscape of AI (ICSCAI), Greater Noida, India, 2024, pp. 1-4.
3. Kumar, Y.L., Sireesha, M., Parvathi, E., Gampala, D., Kumar, A.P., Kishore, G.S. (2025). An Enhanced and Robust Steganography and Cryptography Method Using an Embedding Algorithm. In: Bajaj, A., Abraham, A., Mishra, P.M., Ma, K. (eds) Proceedings of the 15th International Conference on Soft Computing and Pattern Recognition (SoCPaR 2023). SoCPaR 2023. Lecture Notes in Networks and Systems, vol 1246. Springer, Cham.
4. G. Shyam Kishore and Hemalatha Rallapalli, "Deep Convolutional Spiking Neural Network Optimized with Coyote Chimp Optimization Algorithm for Imperfect Channel Estimation in MIMO-fOFDM/FQAM Based 5G Network. International Journal of Intelligent Engineering & Systems 16.3 (2023)."
5. G. Shyam Kishore and Hemalatha Rallapalli, "HFQAM-Based Filtered OFDM: A Novel Waveform Design with Hybrid Modulation for Next-Generation Wireless Systems" Lecture Notes in Networks and Systems, Volume 204, 2021.
6. G. Shyam Kishore, H. Rallapalli, "Towards 5G: a survey on waveform contenders". in ed.by S. Satapathy, K. Raju, K. Shyamala, D. Krishna, M. Favorskaya, Advances in Decision Sciences, Image Processing, Security and Computer Vision. Learning and Analytics in Intelligent Systems, vol 4. (Springer, Cham, 2020)
7. G.S. Kishore, H. Rallapalli, "Performance assessment of M-ary ASK, FSK, PSK, QAM and FQAM in AWGN channel". in 2019 International Conference on Communication and Signal Processing (ICCSP), Chennai, India, pp. 0273–0277. (2019).
8. G.Shyam Kishore, P.Mounika, "Implementation of PRPG with Low-Power BIST", in 2016, International Journal of Innovative Research in Computer and Communication Engineering, vol-4, issue-7 pages:14352-14356.

9. G.Shyam Kishore, K.Tejasvi, “Low-Power and Area-Efficient N-Bit Carry-Select Adder”, in 2016, International Advanced Research Journal in Science, Engineering and Technology, vol-3, issue-7 pages:186-189. DOI:10.17148/IARJSET.2016.3738
10. G. Shyam Kishore, S. Jaya Prakash, B. Sachin, D. Puneeth, “Design Wallace Tree Multiplier Using Reversible Gates”, IJRASET, vol 12, issue 4, 2321-9653, DOI Link: https://doi.org/10.22214/ijraset.2024.60154.
11. G. S. Kishore, K. K. Murthy, P. Vamshika, and S. K. Shinde, “Area-Efficient AES Design for IoT Devices”, IJMDES, vol. 2, no. 12, pp. 28–33, Apr. 2024, doi: 10.5281/zenodo.10968595.
12. G.Shyam Kishore, M Srilatha, “A Comparative Analysis of Look Ahead Clock Gating Using 22nm Technology” in 2015, International Journal of Engineering & Science Research, Vol-5, Issue-7, pages: 654-658.
13. G.Shyam Kishore, G Swetha, “Area-Delay Efficient Implementation of SQRT-CSLA” in 2015, International Journal of Computer Science and Mobile Computing, Vol-4, Issue-7, pages: 50-54
14. G.Shyam Kishore, published paper titled “Design of Low-Voltage Low-Power Comparator Using CMOS Technology ” IJESC Aug 2015, page:1666-1670
15. G.Shyam Kishore, published paper titled “Design and Implementation of Rijndael Encryption Algorithm Based on FPGA” International Journal of Computer Science and Mobile Computing(IJCSMC) sep 2013,vol 2 Issue 9, page:120-127
16. G.Shyam Kishore, published paper titled “ A Novel high seed glitch free D Flip-Flop ” International Conference on VLSI & NEMS (VMN--2012)24-25 Jan 2012, page:95-98
17. G.Shyam Kishore, published paper titled “ A Novel Full Adder with high speed low area” second NCICT- 2011, proceedings published in International Journal of computer Architecture (IJCA) 14-15 Sep 2011, page:34-37.
18. M. Srilatha, G. K. Shyam, “A comparative analysis of lookahead clock gating using 22nm technology”, International Journal of Engineering & Science Research, July 2015, pp 654–658.
19. Gopu S, Kishore GS. Monitoring of home & activation of automated system via GSM through FPGA. Int J New Trends Electron Commun IJNTEC. 2014;2(1):11–14. ISSN:2347-7334.
20. Kadarla Ramyateja et al (2016), “Greenhouse Monitoring and Controlling Using Arm”, International Journal of Computer Science and Mobile Computing, Vol.5, Issue.8, pp. 32-37.

Workshops:

- I have attended a Faculty development program on “Blockchain Technology”, organized by D.Y.patil deemed to be university, bishop heber college and SR university in collaboration with ExcelR Edtech pvt ltd., from 8th – 12th January 2024.
- I have attended a Faculty development program on “Building Advanced Data Analytics with Cloud”, under Next Gen Employability Program, from 18th – 22th December 2023.
- I have attended a Faculty development program on “MASTER CLASS ON MACHINE LEARNING (30 DAYS)”, Pantech Prolabs India Pvt Ltd, from 21st Nov–20th Dec ,2023.
- I have attended a Faculty development program on “Machine learning applications in Micro-Nano VLSI Technologies”, organized by CMR College of Engineering and Technology, Hyderabad, from 24th – 29th April 2023.
- I have attended a Faculty development program on “Li-Fi Technologies and applications”, organized by CMR College of Engineering and Technology, Hyderabad, from 16th – 21st January 2023.

- I have attended a Faculty development program on “IOT in 5G Technology”, organized by CMR College of Engineering and Technology, Hyderabad, from 17th – 22nd October 2022.
- I have attended a Faculty development program on “Advanced Electromagnetics and Modern Antenna Design principles”, organized by CMR College of Engineering and Technology, Hyderabad, from 22nd – 27th August 2022.
- I have attended a Faculty development program on “MATLAB MASTER CLASS(30 DAYS)”, at Pantech Prolabs India Pvt Ltd, from MAY 19-JULY 2,2022.
- I have attended a Faculty development program on “MASTER CLASS ON ARTIFICIAL INTELLIGENCE (30 Days)”, at Pantech Prolabs India Pvt Ltd, from May 9-June 7,2022.
- I have attended a Faculty development program on “Analog and Mixed Signal Design”, organized by CMR College of Engineering and Technology, Hyderabad, from 18th – 23rd April 2022.
- I have attended a Faculty development program on “Applications of Deep Learning to 5G Wireless Communication Technologies”, organized by VelTech Rangarajan Dr. Sagunthala R&D Institute of science and technology, Chennai, from 8th –12th feb 2022.
- I have attended a Faculty development program on “Applied Machine Learning, AI & Its Applications using Python”, organized by EduxLabs in association with E-cell IIT Hyderabad, from 20th Dec 2021 – 6th Jan 2022.
- Attended in short term training program on “Hands on Project Based Approach of 5G Design and Development “(Phase -II) sponsored by AICTE and organized by Department of ECE, Kakatiya Institute of Technology & Science, Warangal, during 14th – 19th December 2020 with ‘A’ grade in Comprehensive exam.
- I have attended “Intensive Internship Program for Faculty on LABVIEW Fundamentals with CLAD Certification”, from 16th – 20th December 2019 at Techfluent Solutions Private Limited, Hyderabad.
- I have attended the Mini-Project Course in Hyderabad on “MU-MIMO, Massive MIMO and OFDM Technologies for 5G Networks” from March 27th - 30th, 2019 at ECE department, UCE, Osmania University, Hyderabad organized by IIT Kanpur.
- I have attended a Two-week GIAN course on "Evolution of Wireless Communication towards 5G" from 07-05-2018 to 17-05-2018, at IIT KHARAGPUR.
- I have attended a Two-week GIAN course on "Next Generation MIMO and OFDM Wireless Technologies" from 08-12-2017 to 17-12-2017, at NIT KURUKSHETRA.
- Attended One Week Faculty Up-gradation Program (FUP) on “Digital VLSI system design using Verilog HDL" from 18-01-2016 to 22-01-2016 conducted by C-DAC Hyderabad in collaboration with TASK (Telangana).
- Attended Two Week ISTE Main Workshop on “Analog Electronics" from 4/6/2013 to 14/6/2013 conducted by IIT Kharagpur.
- Attended two-week AICTE sponsored sponsored staff development programme on “Low Power VLSI Design” by Rajiv Gandhi Memorial College of Engg. & Tech., Nandyal, kurnool, Andhra Pradesh, India, from 18-05-2011 to 31-05-2011.
- Attended one-week Mission 10X workshop organized by Mission 10x, WIPRO from 03-05-2011 to 07-05-2011.
- Attended two-day workshop on “Partial Reconfiguration” organized by XILINX INC. and Dept of CSE, IIT Madras, Tamilnadu, India on 3rd & 4th Jan 2008.
- Attended three-week UGC sponsored Refresher Course on “VLSI Design & Embedded Systems” by JNTU Hyderabad, Andhra Pradesh, India, from 17-11-2004 to 07-12-2004.